## **LAB 3**

## OBJECTIVE: To design and simulate a NOT gate using VHDL, and verify its functionality using a testbench.

## TOOLS USED:

* VHDL (VHSIC Hardware Description Language)
* <https://www.edaplayground.com/> (for simulation)

**THEORY:**

The aim of this lab is to create a NOT gate in VHDL and simulate it using a testbench. The design code describes the logic of the NOT gate, and the testbench applies both possible input combinations to validate the behavior of the gate.

## VHDL CODE

**DESIGN:**

library ieee;

use ieee.std\_logic\_1164.all;

entity notgate is

port( a: in std\_logic;

c: out std\_logic);

end andgate;

architecture behavior of notgate is

begin

c <= not a;

end behavior;

**TESTBENCH**

library ieee;

use ieee.std\_logic\_1164.all;

entity notgate\_tb is

---> no content

end notgate\_tb;

architecture test of notgate\_tb is

component notgate

port(a: in std\_logic;

c: out std\_logic);

end component;

signal ak,ck: std\_logic;

begin

and\_gate: notgate port map(a=>ak,c => ck );

process begin

ak <= '0'; wait for 1 ns;

ak <= '1'; wait for 1 ns;

assert false report "Completed successfully";

wait;

end process;

end test;

Output:



CONCLUSION:

The NOT gate was successfully simulated. The output matched the expected behavior where ck is the inverse of ak for all input combinations. The use of a simple testbench allowed for effective verification of the circuit behavior in a VHDL simulation environment.